Inspecta-5 Hardware

User manual

Inspecta-5 - Hardware
Valid for Inspecta-5 Frame Grabber
Revision 1.1

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INHALTSVERZEICHNIS

1 Preface

This manual describes the High Performance Full Camera Link™ Frame Grabber **Inspecta-5** Hardware.
Inspecta-5 Features :

- Frame Grabber for digitsl cameras with „Full“ Camera Link® Interface.
- Two 26-pin connectors with „Full“ Camera Link® specification for videodata, cameracontrol and und serial interface.
- Videodatarate up to 660 Mbyte/sec.
- Up to 1 GB On-Board memory for fast video.
- PCI-X Businterface with 64 Bits @ 66 MHz clock.
- Maximum datarate on the PCI-X Bus of 528 Mbytes/sec.
- SDK for Windows® 2000/XP
- Four optocoupled in,- and outputs, eg.: external trigger and encoder signals.

Visit www.mikrotron.de for latest Inspecta-5 drivers & tools.

1.1 Scope of this manual

This manual is written for the experienced system user. It describes Inspecta-5 hardware.

Information presented in this publication has been carefully checked for reliability; however, no responsibility is assumed for inaccuracies. The information contained in this document is subject to change without notice.

1.2 Trademarks

2 Installation

2.1 PCI – PCI-X

Inspecta-5 frame grabbers can be used in a 64-bit PCI-X slot with 66MHz @ 532 Mbytes/sec maximum bandwidth or in a standard 32-bit PCI slot with < 132 Mbytes/sec.

2.2 Setup CD

The Inspecta-5 device driver is written for Windows™ 2000/XP. Inspecta-5 is delivered together with a setup CD with the latest driver version, a software manual I5-Level1 and an example project in “C” for Microsoft Developer Studio 6.

See also www.mikrotron.de for newest drivers.

3 Technical Data

Video-Input	80-Bit with up to 10-Taps and/or 8 ore more bits depth.
Videodataformat	„Base“, „Medium“ oder „Full“ Camera Link(R) – compatible.
Videobandwidth	Up to 660 MBytes/Sek.
Imagesize	Random selection of image size horizontal linelenght must be modulo 8.
Onboard memory	Up to 1 Gbyte.
Host - transfer	64-Bit, 66MHz Bus Master burst DMA transfer with scatter-gather capability.
Transferrate	> 400 MByte/s
Cameracontrol-outputs	4 programmable outputs for asynchronous shutter, read out timing oder camerasynchronisation etc. (CC1..CC4).
External signal I/O	4 Ein-/ Ausgänge, optogekoppelt, z.B. für externes Trigger- oder Encodersignal
Powersupply	+3.3VDC / 2,5 A+5V / 0,25 A
Ambient temperature	0 - 50 °C

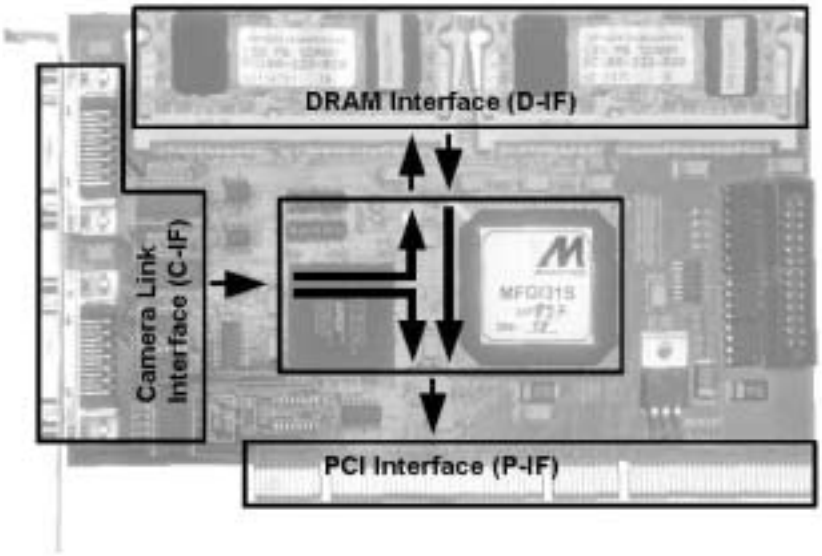
4 Functional description

An essential feature of Inspecta 5 is its on-board memory. Through this memory there is not only one datasource (camera) and one datadestination (PCI-Bus), but an additional source and destination – the up to 1GB large DRAM. All soruces and destinations can be connected to each other. Fifo supported DMA channels do this job.

The interfaces are named accordimg to their function and can be seen on the below schematic:

C-Interface (Camera) – only datasource, 80 Bit
D-Interface (DRAM) – source and destination, 64 Bit
P-Interface (PCI) – destination for videodata, 32/64 Bit

These interfaces, especially their datapaths (C2D, D2P, C2P) are reflected in the driver software.



4.1 Optocoupled I/O

The parallel I/O Port is accessible via a 26-pin male header on Inspecta-5. This header is connected with flat cable to a 25-pin male Sub-D connector on a PC-bracket.

The below table shows the pinning:

25-pol Sub-D connector on the PC-bracket	26Pin Header on Inspecta-5	Name	Description
1	1	nc	
2	3	C2	(Collector PPOut2)
3	5	E2	(Emitter PPOut 2)
4	7	C3	(Collector PPOut3)
5	9	E3	(Emitter PPOut 3)
6	11	nc	
7	13	nc	
8	15	nc	
9	17	nc	
10	19	A0	(Anode PPIn0)
11	21	K0	(Kathode PPIn0)
12	23	K1	(Kathode PPIn1)
13	25	A1	(Anode PPIn1)
14	2	E1	(Emitter PPOut1)
15	4	C1	(Collector PPOut1)
16	6	E0	(Emitter PPOut 0)
17	8	C0	(Collector PPOut0)
18	10	nc	
19	12	nc	
20	14	nc	
21	16	nc	
22	18	A3	(Anode PPIn3)
23	20	K3	(Kathode PPIn3)
24	22	K2	(Kathode PPIn2)
25	24	A2	(Anode PPIn2)
26	-	-	

For all four inputs, the anodes and cathodes of the optocouple LEDs are accessible, just as the emitters and collectors of the four output optocouplers.

There are no additional components on the I/Os besides the optocoupler pins. If, because of excessive overvoltage and/or reversed voltage a coupler breaks, they can be easily replaced because they are socketed.

4.1.1 Optocoupler technical data

Typ	Current transfer ratio	Isolation Voltage	Diode Forward Current	Diode Reverse Voltage	Transistor Collector Current	Transistor Collector Voltage	Bandwidth
ILD30 Opto-Out	>100%	6000V	50 mA	3V	125mA UCE 10V	30V	-
HCPL2531 Opto-In	27% typ 19% min	2500V	16mA	5V	TTL level		3 Mhz

4.1.2 Input wiring (e.g.: light barrier) with NPN-transistor

The following schematics shows the wiring:

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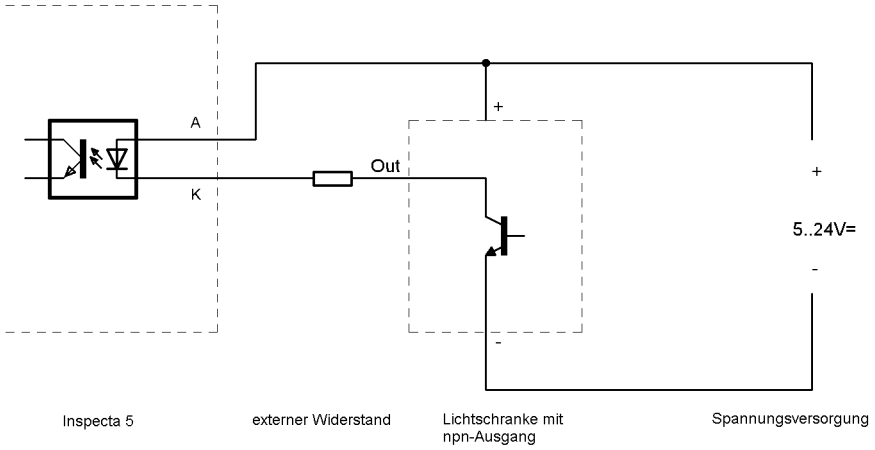
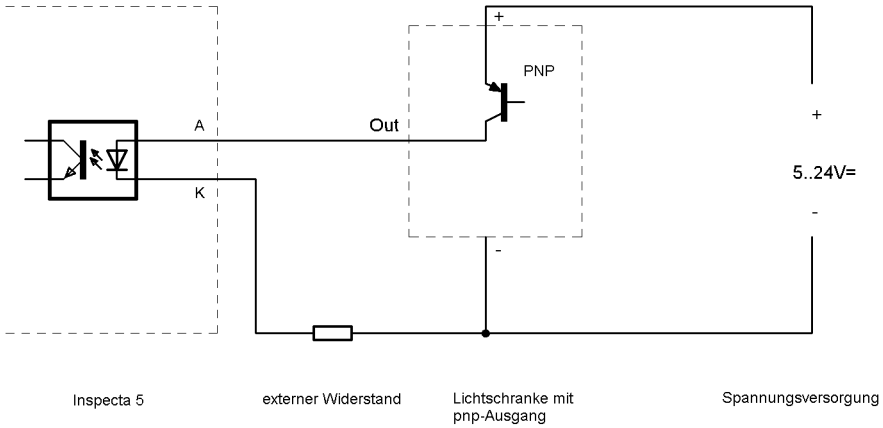


OK1 is the optocoupler on Inspecta-5; R1 and the transistor (e.g.: the light barrier containing this transistor enthält) are external components.

R1 has to be calculated so that the LED current is between 10..16mA: R1 = (U-3V) / 16 mA

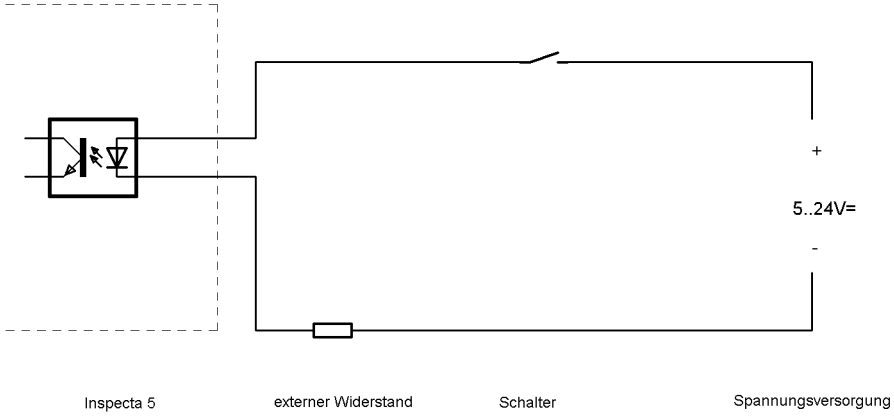
e.g.: U=24V: R1 = (24V - 3V) / 16 mA = 1,3125 kOhm (chosen: 1,5 kOhm)

4.1.3 Input wiring (e.g.: light barrier) with PNP-transistor



Calculation of R1 as above with NPN Transistor.

4.1.4 Input wiring with a switch and an external voltage source



Calculation of R1 as above with NPN Transistor.

4.1.5 Input wiring with an external 5V TTL signal

Make sgure that the external signal can source the LED minimal current (>10mA). Use R1 also.

4.2 Triggerlogic

Inspecta-5 triggerlogic is build with two programmable 32-bit timers (TimerA, TimerB). Each timer uses a clock to count and a startsignal to begin counting. The clock can be either an internal 7,3728MHz clock, or the LVAL signal from the attached camera. Each timer provides an output pulse with a width proportional to the counters clock frequency end the programmed count value. The inputs and outputs of each counter can be connected to several I/O pins (PPIN1..4, CC1..CC4) and to eachother.

There are keywords defined for the configuration of the triggerlogic. These Keywords are used in a “cameraprofile”, e.g.: a camera specific section of the Inspecta-5.cam file.

Description of the keywords in the following table:

Keyword	Parameter	Comment
TimerAStart	SWTrigger Ppin0..3 Quaddec TimerAEnd TimerBEnd	Start signal for TimerA
TimerBStart	SWTrigger Ppin0..3 Quaddec TimerAEnd TimerBEnd	Start signal for TimerB
TimerA|B|C|DClock	 PrescalerOut LvalEdge	Clock source for all Timers: Timebase = 7,3728 MHz / PrescalerABCD Timebase = LineValid Signal
TimerACount	2**32-1..1	32 Bit Downcounter
TimerBCount	2**32-1..1	32 Bit Downcounter
PrescalerABCD	1-255	Prescaler set for TimerABCD count
TriggerSync	No Lval	 Syncs CC with LineValid
LvalEdge	Rising Falling	Lval = LineValid
CC1Source	Ppin0..3 TimerA CCNop TimerC TimerD	Possible Signal sources for CameraLink control CC1
CC2Source	Ppin0..3 TimerA CCNop TimerC TimerD	Possible Signal sources for CameraLink control CC2

Keyword	Parameter	Comment
CC3Source	Ppin0..3 TimerA CCNop TimerC TimerD	Possible Signal sources for CameraLink control CC3
CC4Source	Ppin0..3 TimerA CCNop TimerC TimerD	Possible Signal sources for CameraLink control CC4
CC4..1Polarity	Pos Neg	Level for CameraLink control CC1..4
TimerC|DCount	15..1	Rising/falling edge discriminator for TimerA|B output, edge width
TimerCStart	TimerA rising TimerB rising	Start signal for TimerC
TimerDStart	TimerA falling TimerB falling	Start signal for TimerD
QuaddecDiv	1..255	Quadrature decoder output divider for Quadrature input signals on Ppin1|2

SWTriggerAB	High Low	Triggersignal for SWTrigger. Active with rising edge.

4.2.1 Examples of trigger configuration

4.2.1.1 Pulse width controlled shutter pulse on CC1, triggered with PPIN3

A camera needs a positive pulse on CC1 to start exposure and image output. The width of the pulse is proportional to the cameras exposure time and should 17msec.
The pulse should be issued if optoinput 3 encounters a positive edge.

1.	CC1Source = TimerA	TimerA provides pulse
	CC2Source = NOP	Insure that CC2 is inactive
	CC3Source = NOP	Insure that CC3 is inactive
	CC4Source = NOP	Insure that CC4 is inactive
2.	CC1Polarity = Pos	Pulse must be positive active
	CC2Polarity = Pos	Insure that CC2 is inactive
	CC3Polarity = Pos	Insure that CC3 is inactive
	CC4Polarity = Pos	Insure that CC4 is inactive
3.	TimerABCDclock = Prescale-rOut	Timerclock from internal prescaler
4.	Prescaler = 1	Use 1, more only if width of TimerA|B (32 bits each) is not sufficient
5.	TimerACount = 125338	17ms * 7,3728MHz / Prescaler
6.	TimerAStart = Ppin3	Start Timer1 with PPIN3

4.2.1.2 Pulse width controlled shutter pulse on CC1, retriggered every 58ms

Same as example above, but retriggered not by PPIN3 but internally every 58ms.

1.	CC1Source = TimerA	TimerA provides pulse
	CC2Source = NOP	Insure that CC2 is inactive
	CC3Source = NOP	Insure that CC3 is inactive
	CC4Source = NOP	Insure that CC4 is inactive
2.	CC1Polarity = Pos	Pulse must be positive active
	CC2Polarity = Pos	Insure that CC2 is inactive
	CC3Polarity = Pos	Insure that CC3 is inactive
	CC4Polarity = Pos	Insure that CC4 is inactive
3.	TimerABCDclock = PrescalerOut	Timerclock from internal prescaler
4.	Prescaler = 1	Use 1, more only if width of TimerA|B (32 bits each) is not sufficient
5.	TimerACount = 125338	17ms * 7,3728MHz / Prescaler
6.	TimerAStart = TimerBEnd	
7.	TimerBCount = 427622	58ms * 7,3728MHz / Prescaler
8.	TimerBStart = TimerBEnd	Timer B retriggers itself after 58ms

4.3 Pixel Router

It is possible to connect different types of Camera Link™ cameras to the Inspecta-5. The frame grabber supports cameras with different Taps, 8-14 Bits, colour or black & white.

The type of the camera is set by a parameter in the camera profile (see: Inspecta-5 Software Manual), which configures the Pixel Router of the frame grabber.

Actually this camera types are supported by the Inspecta-5:

Taps	Bits/Pixel	Comment
8	8	Full Camera Link
10	8	Full Camera Link
2	8	Base Camera Link, Port A and B, standard 8-Bit cameras with 2 Taps